FIG. 1, FIG. 3

a··· U-PHASE OUTPUT

b··· V-PHASE OUTPUT

c··· W-PHASE OUTPUT

d··· INVERTER CONTROL CIRCUIT

e··· OUTPUT VOLTAGE COMMAND SIGNAL

f··· PWM PULSE GENERATING CIRCUIT

g··· UP INITIAL SIGNAL

h··· UN INITIAL SIGNAL

i··· VP INITIAL SIGNAL

j··· VN INITIAL SIGNAL

k··· WP INITIAL SIGNAL

l··· WN INITIAL SIGNAL

m··· SIMULTANEOUS SWITCHING PREVENTION CIRCUIT

n··· UP GATE SIGNAL

o··· UN GATE SIGNAL

p··· VP GATE SIGNAL

q··· VN GATE SIGNAL

r··· WP GATE SIGNAL

s··· WN GATE SIGNAL

FIG. 5

a,b,c,d,e··· HIGH-POSSIBILITY SIMULTANEOUS-SWITCHING POINTS

FIG. 6

a··· UP INITIAL SIGNAL

b··· POST-TURNING-OFF Δt_1 GENERATING CIRCUIT

c··· POST-TURNING-ON Δt_2 GENERATING CIRCUIT

d··· SIMULTANEOUS SWITCHING PREVENTION LOGIC CIRCUIT

e··· DEAD TIME GENERATING CIRCUIT

f··· UP GATE SIGNAL

g··· UN GATE SIGNAL

h··· UN INITIAL SIGNAL

i··· VP INITIAL SIGNAL

j··· VP GATE SIGNAL

k··· VN GATE SIGNAL

l··· VN INITIAL SIGNAL

m··· WP INITIAL SIGNAL

n··· WP GATE SIGNAL

o··· WN GATE SIGNAL

p··· WN INITIAL SIGNAL

FIG. 8

A··· GATE DRIVE CIRCUIT